CBCS SCHEME

USN | | | | | | | | | |

15NT34

Third Semester B.E. Degree Examination, July/August 2021
MOSFETs and Digital Circuits

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions.

1 a. Explain transfer characteristic of n-channel JFET. **(06 Marks)**
b. Explain accumulation, depletion and inversion of nMOS enhancement transistor. **(06 Marks)**
c. Discuss Twin-Tub process of CMOS. **(04 Marks)**

2 a. Highlight the advantages of SOI technology. **(06 Marks)**
b. Explain small signal model of MOS transistor. **(06 Marks)**
c. Explain channel-length modulation. **(04 Marks)**

3 a. Explain power dissipation of a CMOS transistor with respect to gate and unit area. **(04 Marks)**
b. Explain MOSFET full scaling and voltage scaling. **(08 Marks)**
c. Explain CMOS inverter. **(04 Marks)**

4 a. Explain the working of CMOS transmission gates highlighting nMOS and pMOS transistor operation. **(08 Marks)**
b. Explain CMOS NAND gate. **(04 Marks)**
c. Explain CMOS 2:1 multiplexer. **(04 Marks)**

5 a. Draw and explain CMOS SR latch by using NAND2 gates. **(06 Marks)**
b. Discuss CMOS implementation of D-latch. **(05 Marks)**
c. By using static AOI gates realize $Y = \overline{(AB + CD)}$ using CMOS technology. **(05 Marks)**

6 a. Explain setup and hold time with respect to CMOS transistor. **(06 Marks)**
b. Explain Schmitt trigger circuit. **(06 Marks)**
c. Explain ring oscillator circuit. **(04 Marks)**

7 a. Explain four bit latch. **(05 Marks)**
b. Explain left-shift, serial in – serial out register by using D flip-flop. **(05 Marks)**
c. Explain the design of Johnson counter. **(06 Marks)**

8 a. Explain mod-4 up/down synchronous counter. **(05 Marks)**
b. Explain mod-8 synchronous up counter. **(07 Marks)**
c. Explain design procedure of synchronous counter. **(04 Marks)**

9 a. Explain Mealy machine and Moore machine. **(06 Marks)**
b. Write a state diagram for 0110 sequence recognizer. **(05 Marks)**
c. Give state diagram for Moore serial binary adder. **(05 Marks)**

10 a. Design a synchronous mod-6 counter using JK flip-flop. **(07 Marks)**
b. Give logic diagram for Melay machine. **(06 Marks)**
c. Define state diagram. **(03 Marks)**

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